REMARKS

The following is intended as a full and complete response to the Office Action mailed on February 07, 2005. Claims 1-35 were examined. The Examiner rejected claims 1-4 and 28-35 of the pending claims under 35 U.S.C. § 102(e) as being anticipated by Heirich (U.S. Patent No. 6,753,878). In addition, the Examiner allowed claims 5-27.

Claim Rejections under 35 U.S.C. § 102(e)

Claim 1 recites the limitations of (i) configuring a multithreaded processing unit of a graphics processor to enable processing of samples independent of the order in which they are received by the multithreaded processing unit and (ii) processing the samples independent of the order in which they are received to render at least a portion of the scene. Heirich does not teach or suggest these limitations.

Heirich discloses an image generator that is organized as a plurality of rendering and a plurality of merge engines. Each of the rendering engines renders a partial image of a scene and provides the partial image to an associated merge engine. The merge engine merges the partial image received from its associated rendering engine with a partial image received from a neighboring merge engine and provides the resulting merged partial image to the next merge engine in the image generator. This "next" merge engine then merges the merged partial image received from the "previous" merge engine with another partial image received from the rendering engine associated with the next merge engine. This sequence continues until a fully rendered image has been generated. The fully rendered image is the ultimate output of the disclosed image generator. See generally Heirich at col. 4, lines 12-29.

Importantly, the image generator disclosed in Heirich is comprised of several separate components that perform the image processing functions described above. For example, the discussion of Figure 1 expressly states that each rendering engine (22) is a standard graphics accelerator card with a PCI interface. See Heirich at col. 6, lines 63-68. Also, pixel bus (28) of Figure 1 is described as a high-speed bus that carries traffic between the different merge engines. The reference calls out the Tandem ServerNet network as a suitable high-speed bus as well as Tandem's ServerNet "Colorado" application-specific integrated circuit (ASIC) as the interface for that high-speed bus. See Heirich at col. 6, lines 20-29 and at col. 7, lines 6-11. In addition, Figure 2 shows the merge engine as a separate system arranged on printed circuit board with a separate ASIC for communicating between other merge engines over a network, such as the ServerNet network. See generally Heirich at col. 7, line 65 – col. 8, line 22. Finally, Figure 6 discloses a graphics processing system (300) or "node" in a network configured to implement the functionality of the image generator described in Figure 1. The graphics processing system (300) includes a separate central processing unit (302), rendering engine chip (310) on a graphics accelerator card (306) and a merge engine chip (320) on a compositing card (308). The description of Figure 6 is very clear that the functionality of the image generator is obtained by networking together several workstations, each of which includes the graphics processing system (300) of Figure 6.

As the foregoing illustrates, the architecture set forth in Heirich is premised entirely upon separate and distinct components carrying out the various functionalities of the disclosed image generator. Therefore, to the extent the system disclosed in

Heirich performs any type of order-independent processing, such processing is being performed by a combination of separate and distinct processing components, not by a multithreaded processing unit in a graphics processor, as recited in claim 1.

By contrast, the method of claim 1 specifically recites the step of configuring a multithreaded processing unit within a graphics processor to perform order-independent processing on the received samples. See, e.g., Figures 1, 2 and 4 of the Application (describing that a multithreaded processing unit (400) carries out processing functionality in each execution pipeline 240). As previous described, the architecture disclosed in Heirich does not teach or suggest in any way that a multithreaded processing unit within a graphics processor is configured to perform order-independent processing.

For these reasons, Applicants contend that Heirich fails to teach or suggest each and every limitation of claim 1. Applicants therefore respectfully submit that claim 1 and claims 2-4, dependent thereon, are in condition for allowance and request withdrawal of the §102(e) rejection of these claims.

Independent claims 28, 30 and 33 recite limitations similar to those discussed above in connection with allowable claim 1 and therefore are in condition for allowance for at least the same reasons as claim 1. Since claims 29, 31-32 and 34-35 depend, respectively, from allowable claims 28, 30 and 33, these claims also are in condition for allowance.

CONCLUSION

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and requests that the claims be allowed. If the Examiner has any questions, please contact the Applicant's undersigned representative at the number provided below.

Respectfully submitted,

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